

*** PRELIMINARY PROGRAM***

- 12:15 – 1:30 p.m. Lunch**
- 1:30 – 1:55 p.m. *Plenary IV: Nanoelectronics -- Revolutionary*
Mark Reed (Yale)
- 1:55 – 2:00 p.m. Discussion
- 2:00 – 2:25 p.m. *Plenary V: Architecture and Systems Integration*
Philip Kuekes (HP Labs)
- 2:25 – 2:30 p.m. Discussion
- 2:30 – 2:55 p.m. *Plenary VI: Fabrication and Manufacturing*
Hank Smith (MIT)
- 2:55 – 3:00 p.m. Discussion
- 3:00 – 3:20 p.m. Coffee Break**
- 3:20 – 5:30 p.m. First Breakout Sessions**

The goals for each of the first breakout sessions are to identify a few key research areas that are potential “Grand Challenges.” Discussions in each breakout session should include “technology pull” (applications) and education. Some writing will be done in each session for possible use in preparing the final report of the Workshop. We anticipate that there will be considerable overlap in the potential Grand Challenges identified by each of the first breakout groups. The following plenary sessions and further breakout sessions are intended to consolidate and refine these concepts into a small number of Grand Challenges in Nanoelectronics.

Session 1. BALLSTON ROOM

Acquiring - sense the environment in real time and transduce the status into processable signals

- Extend range and robustness of chem/bio sensors
- Increased sensitivity
- Diversity for reduction of false positive/negative
- Higher frequency EM response
- Compact arrays
- Close to zero consumed power

Session 2. ARLINGTON ROOM

Storing - memory to store data in non-volatile, compact media

- Bit density
- Read/write speed
- Radiation hardness

Session 3. FAIRFAX ROOM

Processing - logic circuitry to transform rapidly data into information

- Device density
- Speed
- Interconnections (parallel processing)
- Multilevel logic

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Session 4. WILSON ROOM
Transmitting - interconnections to send data rapidly across chip, between chips
and through space
Higher frequency
Wider Bandwidth
Lesser delay
Lower consumed power

Session 5. GLEBE ROOM
Systems Level integration
Mixed signal
Computing algorithms and circuits with potentially defective devices
Architectures for the 'Billion Transistor' chip

5:30 – 6:00 p.m. Breakout Session Leaders Conference, ARLINGTON ROOM

6:00 p.m. Adjourn for day

Thursday, February 12, 2004

8:00 a.m. Coffee

8:30 a.m. Plenary Session (Cont'd), BALLSTON ROOM

8:30 – 8:55 a.m. *Plenary VII: Modeling, Simulation and Design*
Mark Lundstrom (Purdue)

8:55 – 9:00 a.m. Discussion

9:00 – 9:25 a.m. *Plenary VIII: NEMS, Nanosensors and Nanofluidics*
Axel Scherer (Cal Tech)

9:25 – 9:30 a.m. Discussion

9:30 – 9:55 a.m. *Plenary IX: Power and Thermal Management in Nanosystems*
Rama Venkatasubramanian (RTI)

9:55 – 10:00 a.m. Discussion

10:00 – 10:20 a.m. Coffee Break

10:20 – 12:00 a.m. Report Back from 1st Breakout Sessions, BALLSTON ROOM

All participants will hear reports from the first set of breakout sessions and begin the process of collective identification of potential Grand Challenges.

10:20 – 10:30 a.m. Report from Breakout Session 1

10:30 – 10:40 a.m. Report from Breakout Session 2

10:40 – 10:50 a.m. Report from Breakout Session 3

10:50 – 11:00 a.m. Report from Breakout Session 4

11:00 – 11:10 a.m. Report from Breakout Session 5

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11:10 – 12:00 p.m. Discussion: Preliminary Identification of Grand Challenges

12:00 – 1:00 p.m. Lunch

1:00 p.m. – 3:00 noon Second Breakout Sessions

These sessions will discuss each of the potential Grand Challenges, with the goal of defining and describing each one. Some writing will be done in each session for possible use in preparing the final report of the Workshop.

Session 1: BALLSTON ROOM
Session 2: ARLINGTON ROOM
Session 3: FAIRFAX ROOM
Session 4, WILSON ROOM
Session 5, GLEBE ROOM

3:00 – 3:15 p.m. Coffee Break

3:15 – 4:05 p.m. Report Back from 2nd Breakout Sessions, BALLSTON ROOM

All participants will hear reports from the first set of breakout sessions and begin the process of collective identification of potential Grand Challenges.

3:15 – 3:25 p.m. Report from Breakout Session 1
3:25 – 3:35 a.m. Report from Breakout Session 2
3:35 – 3:45 a.m. Report from Breakout Session 3
3:45 – 3:55 a.m. Report from Breakout Session 4
3:55 – 4:05 a.m. Report from Breakout Session 5

4:05 – 5:30 p.m. **Discussion and Refinement of Grand Challenges**

5:30 – 6:00 p.m. **Plenary Session for Writing Subgroups, ARLINGTON ROOM**

Discussion of format of the report & assignment of individual writing subgroups

6:00 p.m. Adjourn for day.

Friday, February 13, 2004

8:00 a.m. Coffee

8:30 a.m. Report Writing Session NSF ROOM II-595

8:30 – 10:00 a.m. Drafting report

10:00 – 10:15 a.m. Coffee Break

10:15 – 11:30 a.m. Writing groups reconvene as needed

12:00 p.m. Draft Report completed, Workshop adjourns.